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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/704,510	11/06/2003	Visveswar Akella	81674-306319	4075

7590 04/15/2005

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EXAMINER	
TON, DANG T	

ART UNIT	PAPER NUMBER
2666	

DATE MAILED: 04/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/704,510	AKELLA ET AL.	
	Examiner	Art Unit	
	DANG T TON	2666	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/06/2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *34-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *34-57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/6/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

2. The disclosure is objected to because of the following informalities: Applicant should provide an updated copending application number 09/187,760 in page 1 of the specification.

Appropriate correction is required.

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional

rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 34-57 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-24 of U.S. Patent No. 6,697,362. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following formalities:

For claims 34-57, the claims 1-24 of U.S. Patent No. 6,697,362 disclose

a distributed memory switch system, comprising: a plurality of ports including a source port and a destination port, wherein a packet is transmitted from the source port to the destination port; a dynamic random access memory (DRAM) memory pool; and an interconnection stage coupled between the plurality of ports and the DRAM memory pool such that the interconnection stage permits the packet to be sent from the source port to the destination port via the DRAM memory pool, the interconnection

stage further splitting the packet received from the source port into a plurality of equal-sized packet portions for storage in the DRAM memory pool, wherein the interconnection stage comprises a switch stage connected to the plurality of ports, and a memory switch connected to the switch stage and to the DRAM memory pool;

wherein the memory pool is comprised of memory banks for respectively storing the packet portions;

wherein the switch stage comprises a first set of ASICs connected to the plurality of ports;

wherein the switch stage comprises at least one ASIC connected to the plurality of ports;

wherein the switch stage comprises at least four ASICs connected to the plurality of ports;

wherein the switch stage determines addresses in the memory pool for storing the packet received from the source port;

wherein the interconnection stage reconstructs the packet portions retrieved from the memory pool into the packet to be sent to the destination port;

wherein the switch stage forms command signals which are associated with the packet received from the source port;

wherein the memory switch comprises a second set of ASICs connected to the switch stage and to the memory pool;

wherein the memory switch comprises at least four ASICs connected to the switch stage and to the memory pool;

further comprising: a switch engine coupled to the interconnection stage for managing the flow of packets between source ports and destination ports;

further comprising: a table RAM coupled to the switch engine;

an interconnection stage configured to transmit the packets between the ports;

and a dynamic random access memory (DRAM) memory pool coupled to the interconnection stage for storing the packets which are

received from the ports, wherein the interconnection stage splits certain of the packets received from the ports into a plurality of equal-sized packet portions for storage in the DRAM memory pool, the interconnection stage comprises a switch stage connected to the ports and a memory switch connected to the switch stage and to the memory pool;

wherein the switch stage comprises a first set of integrated circuits connected to the ports;

wherein the switch stage comprises at least one integrated circuit connected to the ports;

wherein the switch stage comprises at least four integrated circuits connected to the ports;

wherein the switch stage determines addresses in the memory pool for storing the packets received from the ports;

wherein the interconnection stage reconstructs the packet portions retrieved from the memory pool into the certain packet associated with the packet portions;

wherein the switch stage forms command signals which are associated with certain of the packets received from the ports;

wherein the memory switch comprises a second set of integrated circuits connected to the switch stage and to the memory pool;

wherein the memory switch comprises at least four integrated circuits connected to the switch stage and to the memory pool;

further comprising: a switch engine coupled to the interconnection stage for managing the flow of the packets between the ports;

further comprising: a table RAM coupled to the switch engine; and

wherein the memory pool is comprised of memory banks for respectively storing the packet portions.

Note: see claims 1-24 of the patent number 6,697,362.

Applicant's claims 34-57 merely broaden the scope of copending application 09/256,779 claims 1-24 by eliminating the terms " dynamic random access memory(DRAM)" from claim 1 and claim 13 of the patent. It has been held that the omission of an element and its function is an obvious expedient if the remaining elements perform the same function as before. In re karlson, 136 USPQ 184 (CCPA). Also note Ex Parte Raine, 168 USPQ 375 (bd. App. 1969); omission of a reference element whose function is not need would be obvious to one skilled in the art.

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Mayer et al. (6,233,242) is cited to show a system which is considered pertinent to the claimed invention.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to DANG T TON whose telephone number is 571-272-3171. The examiner can normally be reached on MON-WED, 5:30 AM-6:00 PM and Thur 5:30-9:30 A.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, RAO SEEMA can be reached on 571-272-3174. The fax phone number for the

organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

D. Ton